



SINGLE/DUAL/QUAD PCM BIT SYNCHRONIZER

Model 2265

Features

- ◆ Up to 4 Channels in 2U Box
- ◆ Bit Rates
 - 5 bps to 20 Mbps
 - 5 bps to 40 Mbps (Opt)
- ◆ Performance within 1 dB of theory
- ◆ Advanced Lock Detection
- ◆ Loop Bandwidth Settings from 0.01% to 1.6%
 - Extended LBW (Opt)
- ◆ Accepts NRZ-L/M/S, BiØ-L/M/S, DM-M/S; MDM-M/S
- ◆ Bit Rate Deviation Indication
- ◆ Randomizer/Derandomizer
- ◆ Scrambler/Descrambler
 - CCITT V.35 / V.36
- ◆ Convolution Encoder
- ◆ Viterbi Decoder
- ◆ Frame Pattern Detector
- ◆ Input Signal Status
 - Sync and Signal Loss
 - Measured Input Bit Rate
 - Measured Signal Level
 - Input Data Polarity
- ◆ Signal/Data Quality Status
 - Eb/No Measurement
 - BER / CER Measurement
 - BERT PRN
 - Signal Level Measurement
- ◆ Date Generator/Simulator
 - Serial and QPSK(Opt)
- ◆ Auto Bit-Rate Scan (Opt)
- ◆ OPSK/OQPSK/SOQPSK Resequencer (opt)
- ◆ Remote Control via.
 - RS-232 (Std)
 - Ethernet (Opt)
 - IEEE-488 (Opt)

General Description

The GDP Model 2265 Multi-Channel PCM Bit Synchronizer houses up to 4 high-performance bit synchronizer channels in a 2U chassis. The optimized digital design of this unit affords the highest performance characteristics currently available.

The Model 2265 is capable of maintaining synchronization with the signal of interest down to -3 dB Eb/No at a signal level as low as 100 mVpp. When searching for the signal, acquisition is attainable in less than 50 bits. The unit can maintain synchronization for a period of at least 256 bit periods without a transition.

The standard IRIG randomizer/derandomizer for both forward and reverse sequences is provided. (Other randomizer/derandomizers are available.) CCITT V.35 and V.36 scrambling/descrambling is also provided. A variety of Viterbi decoders are available including R1/2 K7 (Std), R3/4 K7 and R1/3 k7 (please inquire for other FEC options).

To assure synchronization to the intended data stream, the Frame Pattern Detector may be invoked. Up to a 64-bit long pattern is detected. Maintaining synchronization with this pattern at the programmed repetition rate and synchronization strategy produces a lock signal. An Automatic Polarity Correction (APC) mode is also provided for inverted data.

Each of the channels includes up to four Analog inputs. Additional inputs are optionally available for RS-422 and TTL levels. Each channel provides a variety of outputs that include; three independent programmable TTL Coded PCM outputs and one TTL Auxiliary Coded output (4 total), two independently programmable (0, 90, 180 and 270 degree) TTL Clock outputs and one TTL Auxiliary Clock output (3 total), two RS-422 Coded PCM and two RS-422 Clock outputs. Front Panel Monitor BNCs are provided for each channel that include one Selected Input Monitor, one PCM Data Out and one Clock Out

The MD2265 includes several unique features to determine the quality of the data. The first is an Eb/No (Signal Quality) measurement. From this measurement the error rate of the data can be determined. The MD2265 also measures errors in the frame synchronizer pattern as well as errors in the Viterbi stream when these modes are enabled. A bit-error-rate (BERT) function is also provided. This allows link tests in a short loop-back to verify proper operation of the module, or long loop-back to measure performance of the link. An advanced lock detector ensures a solid lock indication for the bit synchronizer.

An Auto Scan feature is available that scans the input for up to 8 combinations of bit rates, input codes FEC and frame patterns (per Bit Sync). When the signal criteria is present, the Bit Sync automatically locks and recovers the data and clock.





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SPECIFICATIONS

Inputs, each Bit Sync

Analog Inputs Up to 4 Inputs per Bit Sync- 50 ohms (optional 75) or High Z
Digital Inputs Differential RS-422 and TTL (Optional)

Performance

Bit Rate Range 5 bps to 20 Mbps (40 Mbps Optional)
Tuning Resolution X.XXXE^N (1≤N≤7)
Input Levels 0.1 V_{p-p} Min., +/- 12 V Max.. (others available)
DC Offsets DC Offset + peak input signal without exceeding Level limits.
AC Offset No degradation up to 100% of input signal amplitude at 0.1% of the bit rate.
Loop Bandwidths 0.01% to 1.6% (Extended LBW Range Optional)
Acquisition Range 2x LBW
Sync Acquisition Threshold SNR 0 dB
Sync Maintenance SNR -3 dB
Sync Acquisition < 50 bits
Sync Retention 256 bits without transitions
Bit Error Rate < 1 dB from theory to 40 Mbps

Features

Input/Output PCM Codes NRZ-L/M/S, BI \bar{O} -L/M/S, DBI \bar{O} -M/S, DM-M/S; MDM-M/S
Randomizer/Derandomizer IRIG 106 forward and reverse (Others Available)
Descrambler CCITT V.35/V.36
Viterbi Decoder R 1/2, K 7 with G1/G2 Swap and G2 Invert, (others available)
Resequencer QPSK/OQPSK/SOQPSK (Optional)
Frame Pattern Detector Up to 64 bits with programmable strategy and APC
Auto Scan (Optional) Searches up to 8 Bit Rate, Code, Frame pattern, FEC sets per Bit Sync
Output Data Polarity Same as Input polarity / inverted.
Output Clock Phase 0, 90, 180 & 270 degrees to 20 Mbps; 0 & 180 degrees 20 Mbps to 40 Mbps
BERT Function Bit-Error-Rate Generator/Error Detector (PRN 11/15) (Optional)

Outputs, each Bit Sync Channel

TTL (Each Channel)- Coded PCM and Clocks (Programmable 0, 90, 180, 270 degrees)
RS422 (Each Channel)- Coded PCM and Clock (Programmable 0, 90, 180, 270 degrees)
Bipolar Tape Output (Each Channel)- +/-1V - Coded PCM
Front Panel Monitor (Each Channel)- Selected Input Monitor, PCM Data Out, Clock Out
Composite Lock Status - Bit Synchronization, Frame Pattern and Viterbi

Signal Quality Status: Presented on Front Panel and Remote Port: Bit Sync Lock, Eb/No, Bit Rate Deviation, Signal Presence, Signal Level, Bit Sync Lock-Loss-Count, and PRN BER/CER

Ordering Information

MD2265-02	Basic Dual Channel Unit (20 Mbps)	OP2265-22	Ethernet Remote Control
MD2265-04	Basic Quad Channel Unit (20 Mbps)	OP2265-40	Special Rear I/O
MD2265-01	Basic Single Channel Unit (20 Mbps)	OP2265-41	Recirculate (NRZ-L & Clk In/ RNRZ Out)
OP2265-01	Operation to 40 Mbps	OP2265-43	BERT Option
OP2265-05	QPSK & OQPSK Support	OP2265-45	Auto Scan Option
OP2265-06	SOQPSK Support	OP2265-70	75 Ohm option
OP2265-07	QPSK & OQPSK & SOQPSK	OP2265-91	Extended Loop Bandwidth Range
OP2265-21	IEEE-488 Remote Control	OP2265-92	Reed Solomon Option

Recognizing that no standard product can meet all the needs of all users, GDP stands ready to provide units tailored to unique applications.

The statements in this data sheet are not intended to create any warranty, expressed or implied. Equipment specifications are subject to change without notice.

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