Series Connected Bit Synchronizers Need Sequentially Increased Loop Bandwidths

This article explains why, when Bit Synchronizers are arraigned in a series configuration with the output of one Bit Synchronizer feeding the input of the next Bit Synchronizer, the second Bit Synchronizer loop bandwidth should be wider than the loop bandwidth of the first Bit Synchronizer.

A Bit Synchronizer is used to recover clock and data from a PCM data source. The PCM data is often corrupted with noise and jitter. As a Bit Synchronizer recovers the clock from noisy PCM data, some of the noise is converted to phase jitter. It is desirable that this noise induced jitter be minimal without any resonant peaks. In addition, the Bit Synchronizer should track any input jitter with minimal jitter gain.

A Phase Lock Loop (PLL) is used as part of the Bit Synchronizer clock recovery algorithm. Even an ideally implemented PLL exhibits some jitter gain near and at the loop natural frequency. This is illustrated in Figure 1. For example, with a damping factor of 0.7 (the damping factor design value used in Bit Synchronizers) there is a 2dB jitter gain at the resonant frequency. This means that, at the resonant frequency, the jitter amplitude coming out of the Bit Synchronizer is 2dB greater than the jitter amplitude going in. If the Bit Synchronizer has less effective damping, for example 0.3, the jitter gain is 6dB. Underdamping and jitter gain result in increased ringing in the PLL response, an increase in bit error rate and, in the worst case, an inability to maintain lock. Cascading Bit Synchronizers, each being set to the same loop bandwidth, exasperates the problem as the jitter gain is additive. If the subsequent Bit Synchronizer is programmed to a wider loop bandwidth than the first, jitter gain from the first Bit Synchronizer is maintained.

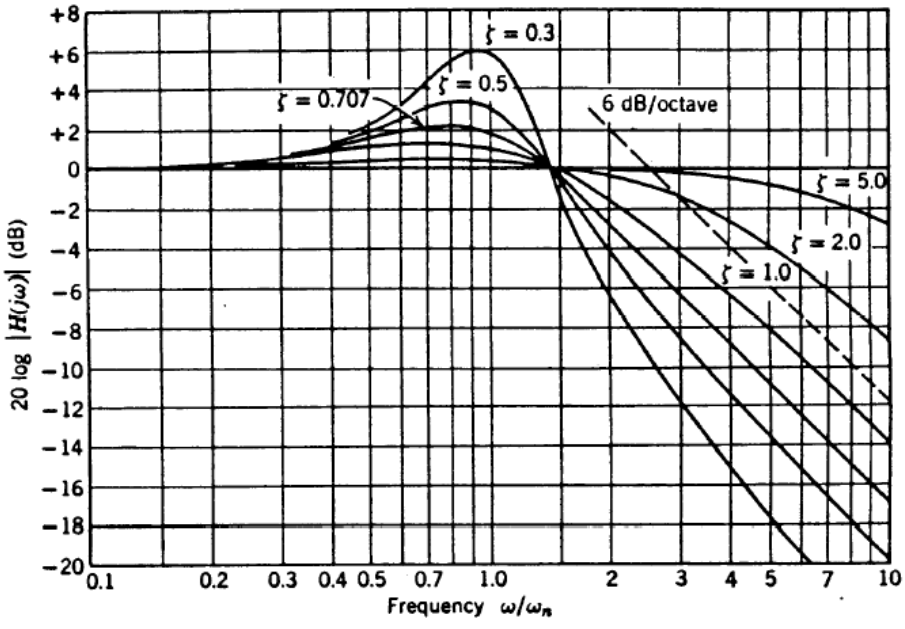

Figure 1 Bit Synchronizer PLL frequency response verses loop damping (from F.M Gardner, Phaselock Techniques, Wiley 1979)

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The actual damping in a Bit Synchronizer is not necessarily the design value. Three main factors affect damping: data transition density, instantaneous signal amplitude, and delay around the phase lock loop. Damping is inversely proportional to the data transition density. The transition density of randomized data is 0.5. If the data is not randomized and has a transition density of 0.25 (for example a "10001000" repeating sequence) the damping is reduced from 0.7 to 0.3. Damping is also inversely proportional to the instantaneous data amplitude. If the data amplitude is varying faster than the Bit Synchronizer AGC can track, the loop jitter gain increases. However, the most surprising degradation is due to delay within the PLL. As the loop delay increases (relative to the inverse of the loop bandwidth) the loop phase margin decreases and loop damping decreases. As a result, the loop jitter gain increases. This may come as a surprise to the user because a 1% loop bandwidth that works fine at 1Mbps may be severely underdamped at 10Mbps because the loop delay relative to the loop bandwidth is now 10 times greater.

It must be recognized that not all Bit Synchronizers are created equal. The jitter response of two Bit Synchronizers is shown in Figure 2. The jitter response curve of the GDP Bit Synchronizer illustrates the expected behavior of a well-designed Bit Synchronizer. Acceptable jitter performance is found in the area below the curve. The GDP Bit Synchronizer exhibits exceptional performance. It can be seen that large jitter amplitudes below and above the loop natural frequency are tracked. Jitter tolerance is reduced for jitter frequencies near the loop natural frequency. However, the 'other' Bit Synchronizer cannot tolerate nearly as much jitter for any jitter frequency below the Bit Synchronizer loop natural frequency. Even with a wider loop bandwidth setting the 'other' Bit Synchronizer cannot track the output of the GDP Bit Synchronizer for large jitter amplitudes.

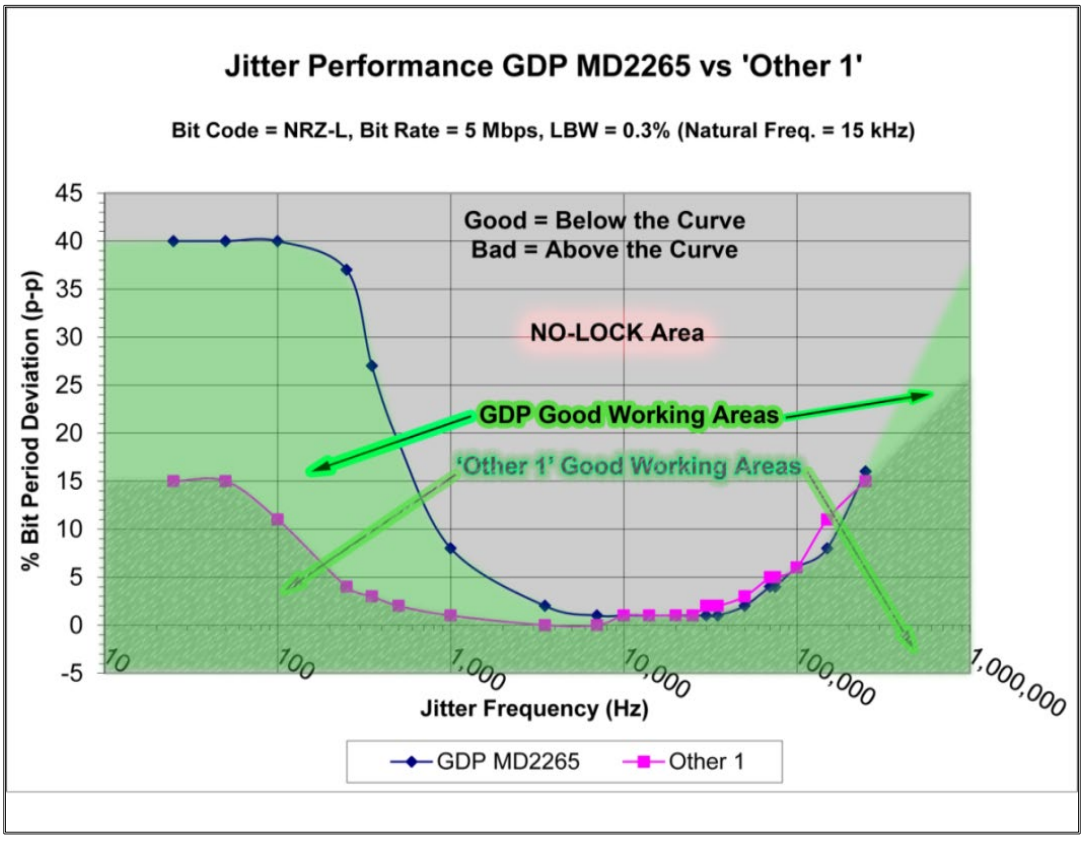

Figure 2 Bit Synchronizer Jitter Performance

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Figure 3 clearly demonstrates the need to increase the loop bandwidth of the second Bit Synchronizer in a series configuration. For this test the data rate is 1Mbps. The first Bit Synchronizer loop bandwidth is set to 0.3%. The input data transition density is only 10%. The jitter rate is set to 300Hz. Figure 3 clearly illustrates that the second Bit Synchronizer loop bandwidth must be set wider than the loop bandwidth of the first Bit Synchronizer so that the second Bit Synchronizer can maintain synchronization and track the output of the first Bit Synchronizer. If the second Bit Synchronizer loop bandwidth is set less than the first Bit Synchronizer loop bandwidth the second Bit Synchronizer does not track the jitter.

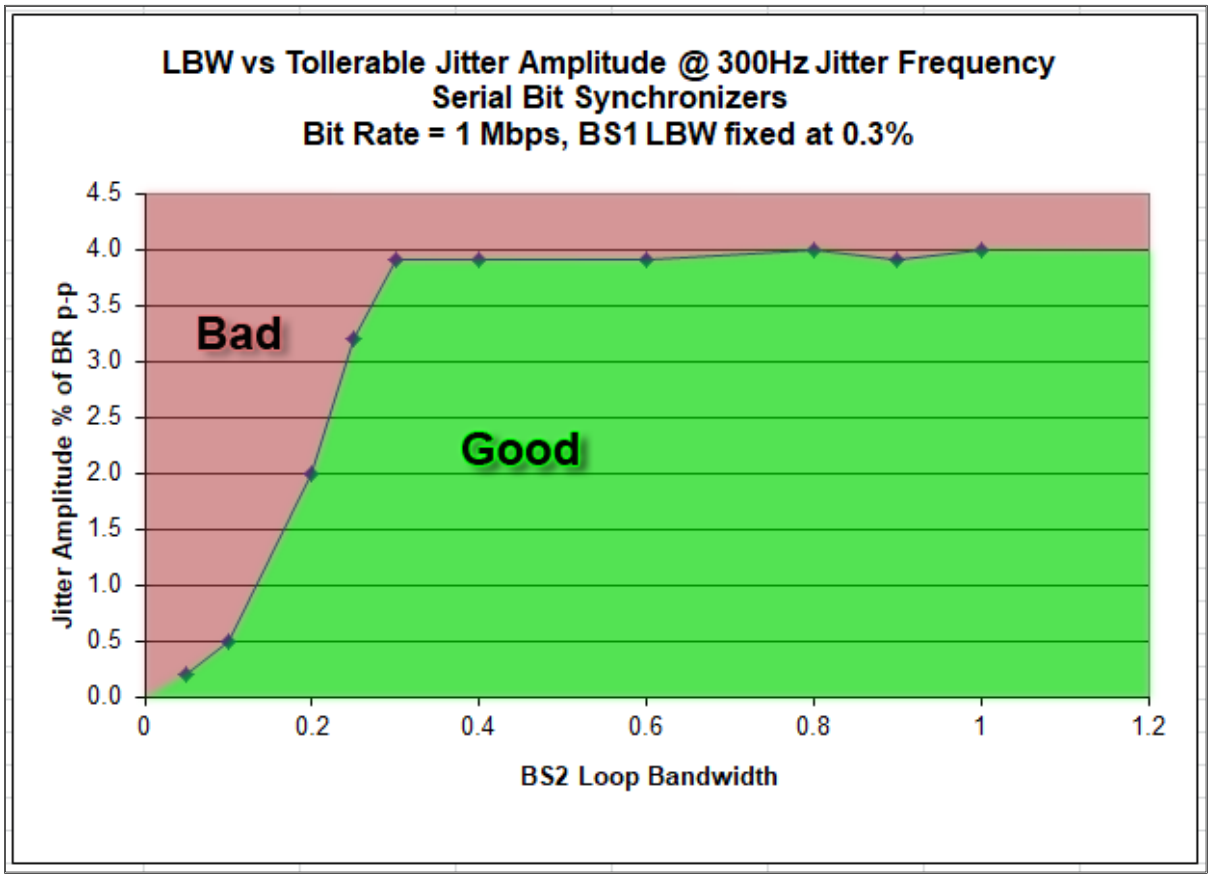

Figure 3 Series Bit Synchronizer Jitter Performance

The GDP Model 650 Data Transition Test Set has a jitter performance measurement feature that measures and plots the jitter performance of a bit synchronizer. It can also be used with many modulators/transmitters to measure and plot Receiver jitter tolerance.

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