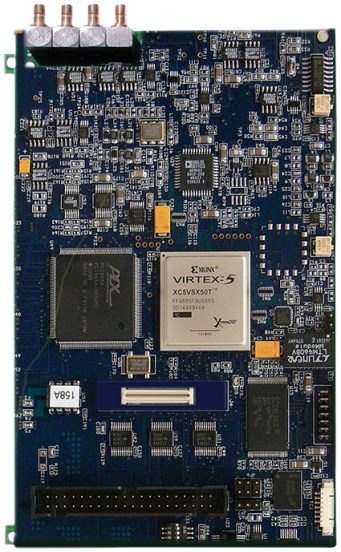
40 MHz advanced PCM Bit Sync Mezzanine

Model 474DM

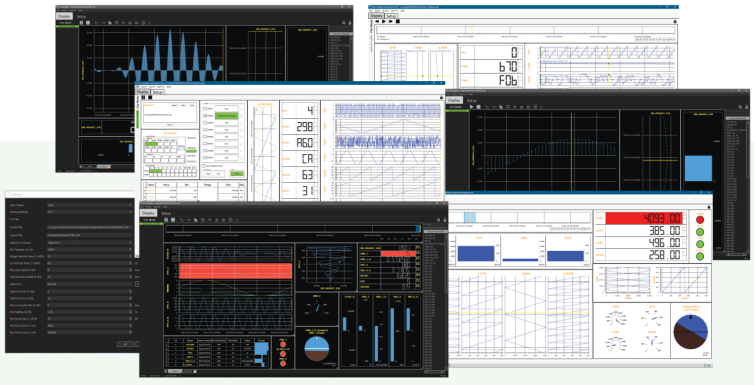
- Bit Rate Range, all codes
  - 8 bps to 40Mbps, standard
- Best-in-Class Noise Performance
- within 0.50 db of theoretical
- Fast sync acquisition
  - within 50 bit transitions, typical
- Best in Class Sync Retention
  - to 1024 bits without transition
- Data Quality and Signal Test:
  - BERT / PRN BER Link Test Mode
  - Frame Sync PCM BER Monitor
  - Frame Lock/Loss Monitor
  - Eb/No Signal Quality Output
  - Viterbi Error Monitor / Stats
  - Data Simulator/Generator
- Processes all IRIG Codes Remote Software Operations
  - The GUI Setup & Operation status of all Acroamatics Bit Syncs are controlled via a single interface, with drop down menus for individual cards. The software automatically recognizes all available bit syncs & their features. Up to 20 unique setups are stored and available for instant bit sync config., supporting from 1-64 bit syncs apps.



The Model 474DM Advanced Digital PCM Bit Sync is a state-of-the-art compact “mezzanine” design that provides a cost effective and modular high quality bit sync add-on to Acroamatics entire line of single slot PCI single card telemetry processing card products.

The 474DM is compatible with both existing legacy and our latest leading-edge design telemetry card components. Based on our latest (3rd generation) bit sync design, it shares the latest techniques in FIR filtering, digital phase-locked loop, NCO clock reconstruction, and digital amplitude and offset control with it’s larger PCI cousin, the Model 1611P.

Incorporating a leading-edge FPGA, the modern design delivers a greatly reduced parts count, improved reliability, and expanded capabilities - including options normally found only in box level and multi-card bit sync/ encoder designs. The 474DM supports options such as Frame Sync Pattern Verification, BERT, PRN and programmable PCM simulator, and Convolutional encode/decode.



Acroamatics Telemetry Software Suite (ATSS)

Acroamatics’ TDP family of products are delivered with Acroamatics Telemetry Software Suite (ATSS). ATSS offers superior data imaging, analysis, and system operations tools. This powerful operating system independent software package provides an extensible environment for setup and control of the TDPSS as well as recording, playback, real-time quick-look display, and precise post system analysis of the acquired telemetry measurement data.

The ATSS can be delivered for use on either a 64-bit Windows 10 (Secure Host Baseline validated) or Red Hat Enterprise Linux 7 Acroamatics telemetry processing platforms allowing the TDPSS system to be tailored to the customers preferred OS environment. Applicable DISA STIGs are applied and support is available to maintain compliance with the latest cyber security requirements. Acroamatics’ high-performance telemetry processing solutions provide users a winning combination of unique architectural and functional advantages.

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40 MHz advanced PCM Bit Sync Mezzanine

Model 474DM

ACROAMATICS
TELEMETRY SYSTEMS

Signal Inputs

Source	Two Inputs, Operator Program selectable
Isolation	Greater than 60dB at 20MHz
Impedance	Program selectable: Hi-Z/Lo-Z. Single Ended: 4kΩ/75Ω (std) or differential : 150 Ohm or Hi-Z (opt)
Signal Level	0.2 to 20V p-p, Single-ended. Differential: 0.2 to 10V p-p, Differential (optional)
DC Offset	20V max, Single-ended Hi-Z or 15V Max @ 75Ω.
Baseline Variation	Tracks sinusoidal offsets to 100% p-p signal amplitude at 0.1% bit rate
PCM Codes	Program selectable: NRZ-L/M/S, Biø-L/M/S, DBiø-M/S, DM-M/S, MDM-M/S, RZ
Derandomizer	Program selectable: RNRZ 9/11/15/17/23, forward/revers

Synchronization

Bit Rate Range	8 bps - 40 Mbps, All PCM Codes
Tuning Resolution	0.1% of bit rate
Capture Range	3 times the programmed loopwidth, typical
Tracking Range	±12% typical, with programmable limiter
Loop Bandwidth	0.1% to 3.2%, program selectable in 0.1% increments
Sync Threshold	0dB for NRZ-L and Biø-L codes
Sync Maintenance	(LW=0.1%) –2dB NRZ-L and Biø-L codes
Sync Acquisition	(LW=1.6%, SNR > 12dB) Typically less than 50 bit periods
Sync Retention	(LW=0.1%, SNR > 3dB) Retains sync through > 1024 consecutive dropouts
Bit Error Rate	(LW=0.1%) to within 0.50 dB of ideal bit error rate performance curves

Data / Clock Outputs, NRZ-L

NRZ-L Data	One each, NRZ-L data/clk pair, RS422/TTL (jumper, selectable) - operator program output selectable to INTERNAL (direct to host decom card via internal bus) or EXTERNAL (output pair directed to card external output BNC or Triax cables)
Data Clock	0º, 90º, 180º, 270º, operator program selectable
Data Polarity	Program selectable: normal/inverted

Data / Clock Outputs, Code (Dual PCM Encoder)

Data Source	Program selectable: Recovered Data (Bit Sync NRZ-L Data/Clk - DEFAULT) or External data/clock (PROGRAM SELECTABLE)
Outputs	Three each: One each TTL data/clk (0º & 180º, selectable) Code (selectable) PCM and Clk, One each TTL data RNRZL, One each TAPE (code selectable) TTL or ±2 Volts balanced output, 50mA drive current
Randomizer	Program selectable: RNRZ 9/11/15/17/23, forward, reverse
PCM Codes	Program selectable: NRZ-L/M/S, Biø-L/M/S, DBiø-M/S, DM-M/S, MDM-M/S, RZ

External Data/Clock PCM Encoder Input

Signal Type	Jumper selectable: RS422 or TTL
Impedance	120Ω RS422, 75Ω TTL
Data Code	Program selectable: NRZ-L/M/S, Biø-L/M/S, DBiø-M/S, DM-M/S, MDM-M/S, RZ
Data Clock	Program selectable: Normal/Inverted, 1x or 2x

Convolution Encoder/Decoder (optional)

Viterbi Decoder	Rate 1/2, k=7: includes differential decoding, V.35 descrambling, and G2 invert (others available)
Symbol Formats	Serial, parallel, and staggered parallel (others available)
Convolutional Encoder	Rate 1/2, k=7: includes differential encoder, V.35 scrambler, and G2 inverter (others available)
Symbol Formats	Serial, parallel, and staggered parallel (others available)

Format Generators/Synchronizer (optional)

Format Generator	Programmable frame length, sync pattern and mask
Synchronizer Source	Recovered data, external data, or test generator
Synchronizer Strategy	Pattern match in “search”, programmable error limits for “check” and “lock” states
Other Features	Bit slip enable, auto polarity enable, data source/ambiguity resolution

Bit Error Rate Tester (optional)

Transmitter Pattern	PRN sequence: PN7, PN9, PN11, PN15 (forward/reverse)
Pattern Clock Source	Program selectable: Bit Rate Clock or External Clock
Blanking	Program selectable: 64, 128, 256 bits
BER Sample Period	Program selectable: 1E3 to 1E9 bit periods, or continuous accumulate
Variable Output	50mV to 5V P-P
Other Features	Automatic pattern synchronization, forced error ON/OFF

Physical

Hosts Supported	Plugs onto Models 1611P, 1626P, 1612P, & 1622P (PCI) and Legacy 1601P, 1602P (PCI) & 1502V (VME) cards, & RS-232.
Cooling Requirements	30 Linear FPM
Power Requirements	+5VDC @ 1.25A, ±12VDC @0.25A
Dimensions	6.5” (16.51cm) H x 4.0” (10.16cm) W x .625” (1.5875cm) D
Temperature	Operating 0 to +40°C, non-operating –40 to +86°C
Relative Humidity	Up to 90% non-condensing
Shock / Vibration	Operating 6G, Non-operating 25G / Operating 0.3G, 5 to 2000 Hz, Non-operating 0.8G, 5 to 500 Hz

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