GDP SPACE SYSTEMS

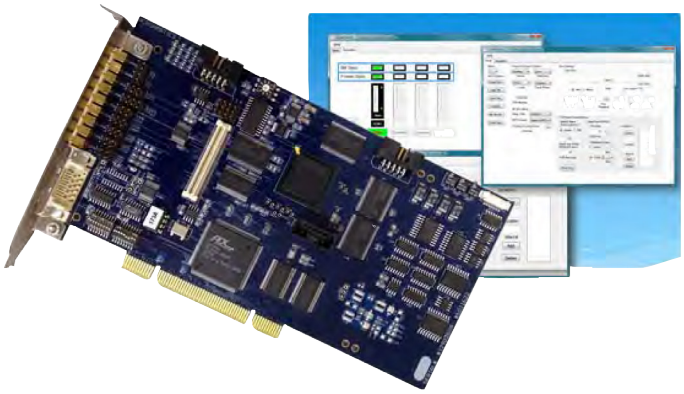
ACROAMATICS
TELEMETRY SYSTEMS

MultiChannel PCM Quick-Look Processor
Model 1626P

Features:

- PCM Frame Sync and “quick-look” Decom
- Programmable 64 Mbps PCM Format Simulator
- IRIG A, B & G Time Code Translator/ Generator
- “all-in-one” quick-look Frame Sync / Decom
- NEW Low latency CVSD PCM-to-DAC analog voice out processor OPTION
- Accepts Model 474DM tunable 40 Mbps Bit Sync
- Available in one to four stream versions
- Well suited for customer raw data recording & post-processing custom software applications
- Individually programmable word properties
- Minor frame lengths up to 64k words & variable frame lengths
- Programmable serializer extracts embedded data
- Auto-double-buffering memory with 512k Byte per stream

General Description



IRIG 106 CVSD Turn-Key Option

We designed the Model 1626P to do basic frame synchronization & decommutation for applications, such as data recording & post-analysis, where powerful embedded frame and word level decom output data formatting for 3rd party post-test or realtime EU processing software is desired.

The 1626P is a 3/4 length PCI-compatible card that can be ordered with from 1 to 4 independent PCM frame sync/decom channels at bit rates up to 64 Mbps. The Model 1626P card includes a powerful onboard PCM Simulator and IRIG Time Code Reader / Generator.

The 1626P accepts Acroamatics new Model 474DM tunable 40 Mbps Bit Sync mezzanine to provide a complete single stream solution in a compact and low cost PCI card format.

Frame lengths of up to 64k words are supported, words are individually programmable as to: length, justification (left or right), orientation (MSB or LSB), suppression, and embedded processing.

Strategy controls allow up to 64-bit patterns, 0-15 allowable errors, +/-3 bit slips, 0-15 flywheel counts, and three sync strategy modes. The card stores data in onboard physical memory with 512k bytes assigned to each PCM stream. The two halves of each 512k block are alternately mapped as they fill with data into a 256k memory space that provides software-transparent fully automatic double-buffering.

Data is available directly from the PCI-bus or can be transferred via the two DMA channels provided. Each record block of data can be a single frame or a programmed record length. Frame status may be inserted into the record,and status read “on the fly”.

An IRIG CVSD standards compliant low latency PCM processing solution is offered as an option within the single stream configuration of the Model 1626,complete with turn-key Windows software set-up and operating software.

FUNCTION

Sources	Available in 1 to 4 channel configurations - each accepting RS-422 0° clock or NRZ-L data or single-ended input data
Impedance	RS-422: 120Ω input impedance, TTL 50Ω input impedance
Bit Rate	Up to 64 Megabits per second
Data Polarity	Programmable with automatic polarity correction
Clock Polarity	Programmable. 0° or 180°
Frame Length	Programmable, 4 to 65536 words

SYNCHRONIZATION

Mainframe Sync	Provides for programmable sync pattern and mask, complement pattern recognition, and variable length frame decommutation. Pattern length up to 64 bits.
Alternate Complement Sync	Synchronizes to formats where the minor frame sync pattern complements on alternate frames
Complement Frame Sync	Synchronizes to formats that complement the minor frame sync pattern at a major frame rate
Automatic Polarity Inversion	Input polarity is inverted when two consecutive complemented sync patterns are found
Sync Modes	Fixed, Adaptive and Burst
Sync Strategy	SEARCH, VERIFY and LOCK
Sync Error Tolerance	0 to 15 errors, programmable
Sync Slip Window	0, ±1, ±2 & ±3 bits, programmable
Clock Rate Monitor	A programmable delay counter returns the synchronizer to SEARCH if the clock input is lost

PCM WORD DECOMMUTATION

The PCM format is decommutated by using the contents of the WORD PROPERTIES MEMORY (which provides one word for each PCM word and one segment for each channel synchronizer) to decommutate the serial data into words. The memory provides the following information for EACH WORD.

General	Bits in this word (from 1 to 32); the orientation of the input data, MSB or LSB first; and if data is right- or left-justified in the output word.
Serializer Enable	Enables the current word to be serialized to extract embedded data.
Suppress Bit	Setting this bit discards the current word from the output record.
Variable Length Frame	Setting this bit accepts the sync pattern at any position of the current word.
End of Frame	Setting this flag recycles the frame at the completion of the current word.

OUTPUT

Output Buffer Size	Double buffered 65,536 32-bit words, for each channel. The data can be read directly from the PCI bus or via the DMA Channels
Header	A header can be inserted at the start of each frame. Header components, Time, Status and Frame number are user selectable.
Time	Time of day in BCD microseconds, as a 64-bit word. If enabled, the time of day will occupy the first two words of a 32-bit output format header
Minor Frame Counter & Frame Status Word	A 32-bit status word can be inserted into the header immediately following the time words. The upper 16 bits contain synchronization status and the lower 16 contain a frame count. Status message reflects H/W status of the previous frame.
Output Format	Data only, no ID tags, and all output words are 32 bits
Output Word Formatting & Justification	16- or 32-bit word selection determines output word formation. The 16 bit format can be used when all PCM words are 16 bit or less. The 16 bit word format packs two right- or left-justified 16 bit words into a 32 bit word. In 32 bit format the PCM words will be right- or left-justified into a 32 bit word.
Host PCM Status	A status word is available for each PCM frame synchronizer via the PCI bus.
Discrete Status	The LOCK status of each frame synchronizer can be output as an RS-422 signal.
Frame Mark	A frame mark can be output as an RS-422 signal

PCM SIMULATOR

Bit Rate	to 64 Mbps
Programming	Automatically copies word and frame attributes from programmed Decom setup or for more sophisticated simulator setups. Text file programming is provided.
Data Sources	1024 Static Registers, Two User-Defined 16 bit Dynamic Data Memories, Two 16-bit Module Up/Down Counters, 16-bit Pseudo-Random Generator, 16-bit Program Counter
Word Lengths	Programmable for each data source; Static data words range from 1 to 32 bits. All other data sources range from 1 to 16 bits.
Word Orientation	Programmable MSB/LSB for each data word
Dynamic Data Memory	2K x 16 bit RAM, Pre-settable to ramp, sine, triangle or square wave functions
Frame Length	Maximum of 4096 words

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PCM SIMULATOR & CLK/DATA OUTPUT

External/Internal	Externally via PCM Simulator clk/data Out. Internally connects to Bit Synchronizer or Frame Synchronizer via program control.
Clock and Data	Zero degree Clock, NRZ-L Data, TTL
PCM Code Type	Sixteen selectable output codes: NRZ-L/M/S, Biø-L/M/S, DBiø-M/S, DM-M/S, MDM-M/S, RNRZ 11 15, 17 and 23

CVSD/DIGITALLY DECODED ANALOG VOICE OUTPUT

Output	600 ohm analog audio voice output, with operator CVSD software program controlled output gain setting
Filtering	Zero degree Clock, NRZ-L Data, TTL
Properties	Individually operator programmable Frame, Digital Audio Word, and Waveform Decoding properties per IRIG-106

IRIG TIME CODE READER/GENERATOR

Functional

Amplitude	0.5 to 20 Vpp, Single-ended
Impedance	12K Ohms minimum
Input Codes	Translates IRIG G, A, and B
Input Frequency	125 Hz to 400,000 Hz
Modulation Index	2:1 through 5:1.
Polarity	Program selectable, Invert or Normal Polarity
Internal	40MHz Crystal Oscillator

Operational

Generate Mode	Time is generated from the onboard crystal oscillator and is pre-settable from the Host.
Translate Mode	Time is read from an external source.
Translate Carrier Mode	The internal timing is based on the input carrier. This mode enables the system to translate time as the input carrier rate varies during playback of an analog recording
Translate Failsafe Mode	The internal timing is phase-locked to the input carrier. In the event of time dropout, the translator continues generating time without interrupt.
Frame Bypass	Automatic frame bypass compares previous time frame with current one, and Time Accumulator updated when they agree.

BIT SYNCHRONIZER OPTION

MODEL 474DM ADVANCED DIGITAL BIT SYNCHRONIZER MEZZANINE

The Acroamatics Model 474DM is a range quality 8 bps to 40 Mbps tunable bit sync daughter card designed specifically for use with the Model 1626P single card TM solution. Please refer to the 474DM data sheet for detailed specifications.

Physical

Format	Standard PCI: 3/4 length single slot
Cooling Requirements	30 Linear FPM
Power Requirements	+3.3VDC at 600mA max, +5VDC @ 600ma max, ±12VDC @ 20mA
Power Requirements +5 Version	+5.0VDC @ 1A max, ±12VDC @ 20mA
Dimensions	4.20” (10.67cm) H x 9.4” (23.80cm) W x .55” (1.4cm) D
Temperature	Operating: 0º to +40º C, Non-Operating: -40º to +86º C
Relative Humidity	Up to 90% non-condensing
Shock	Operating: 6G, Non-Operating: 25G
Vibration	Operating: .3G, 5 to 2000Hz, Non-Operating: .8G, 5 to 500Hz

Specifications subject to change without notice.

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